APPENDIX A
FEATURE DETERMINATION

CPUID Instruction

The Military Intel486 processor implements the CPUID instruction that makes information available to the system software about the family, model, and stepping of the processor on which it is executing. Support of this instruction is indicated by the ability of system software to write and read the bit in position EFLAGS.21, referred to as the EFLAGS.ID bit. The actual state of the EFLAGS.ID bit is irrelevant and provides no significance to the hardware. This bit is reset to zero upon device reset (RESET and SRESET) for compatibility with older Military Intel486 processor designs.

Operation

The CPUID instruction requires the software developer to pass an input parameter to the processor in the EAX register. The processor response is returned in registers EAX, EBX, ECX, and EDX.

1. When the parameter passed to EAX is zero, the register values returned upon instruction execution are:

   EAX[31:0] ← 1

   EBX[31:0] ← 756E6547—''Genu'', with ''G'' in the low nibble of BL

   EDX[31:0] ← 49656E69—''inel'', with ''i' in the low nibble of DL

   ECX[31:0] ← 6C65746E—''ntel'', with ''n'' in the low nibble of CL

   The values in EBX, ECX, and EDX indicate an Intel processor. When taken in the proper order, they decode to the string ''GenuineIntel.''

2. When the parameter passed to EAX is one, the register values returned upon instruction execution are:

   EAX[3:0] ← xxxx—Stepping ID

   EAX[7:4] ← xxxx—Model

   EAX[11:8] ← 0100—Family

   EAX[15:12] ← 0000

   EAX[31:16] ← Intel Reserved

   EBX[31:0] ← 00000000

   ECX[31:0] ← 00000000

   EDX[0:0] ← 1—FPU on-chip

   EDX[3:1] ← 1

   EDX[31:4] ← Intel Reserved

   The value returned in EAX after CPUID instruction execution is identical to the value loaded into EDX upon device reset. Software must avoid any dependency upon the state of reserved processor bits.

3. When the parameter in EAX is greater than one, the register values returned upon instruction execution are:

   EAX[31:0] ← 00000000

   EBX[31:0] ← 00000000

   EDX[31:0] ← 00000000

   ECX[31:0] ← 00000000

Flags Affected

No flags are affected.

Exceptions

None.

For More Information

Refer to the Intel application note AP-485, *Intel Processor Identification with the CPUID Instruction* for more details.

Table A-1. CPUID Instruction Description

OPCODE	Instruction	Processor Core Clocks	EAX Input Value	Description
0F A2	CPUID	14 9	1 0 or greater than 1	Processor Identification Intel String/Null Registers

APPENDIX B
I/O BUFFER MODELS

For processor bus speeds above 33 MHz (e.g., 50 MHz), the capacitive derating curves are not guaranteed. For bus speeds of 50 MHz, I/O buffer modeling techniques should be used to accurately simulate (and predict) the behavior of processor signals in a particular environment.

This appendix presents a sample I/O buffer model parameters for the IntelDX4 processor. The first section presents an overview of signal buffer type catagorization. The second section presents a graphical representation of IBIS (I/O Buffer Information Sheet) data for each of the input, input/output, and output buffers types on the processor. The third section provides a text listing of the data presented in the IBIS format.

I/O buffer model information is available for all Military Intel486 processors described in this datasheet. Contact your Intel representative for the latest I/O buffer models for the IntelDX4 and other members of the Military Intel486 processor family.

I/O Buffer Models for IntelDX4 Processor

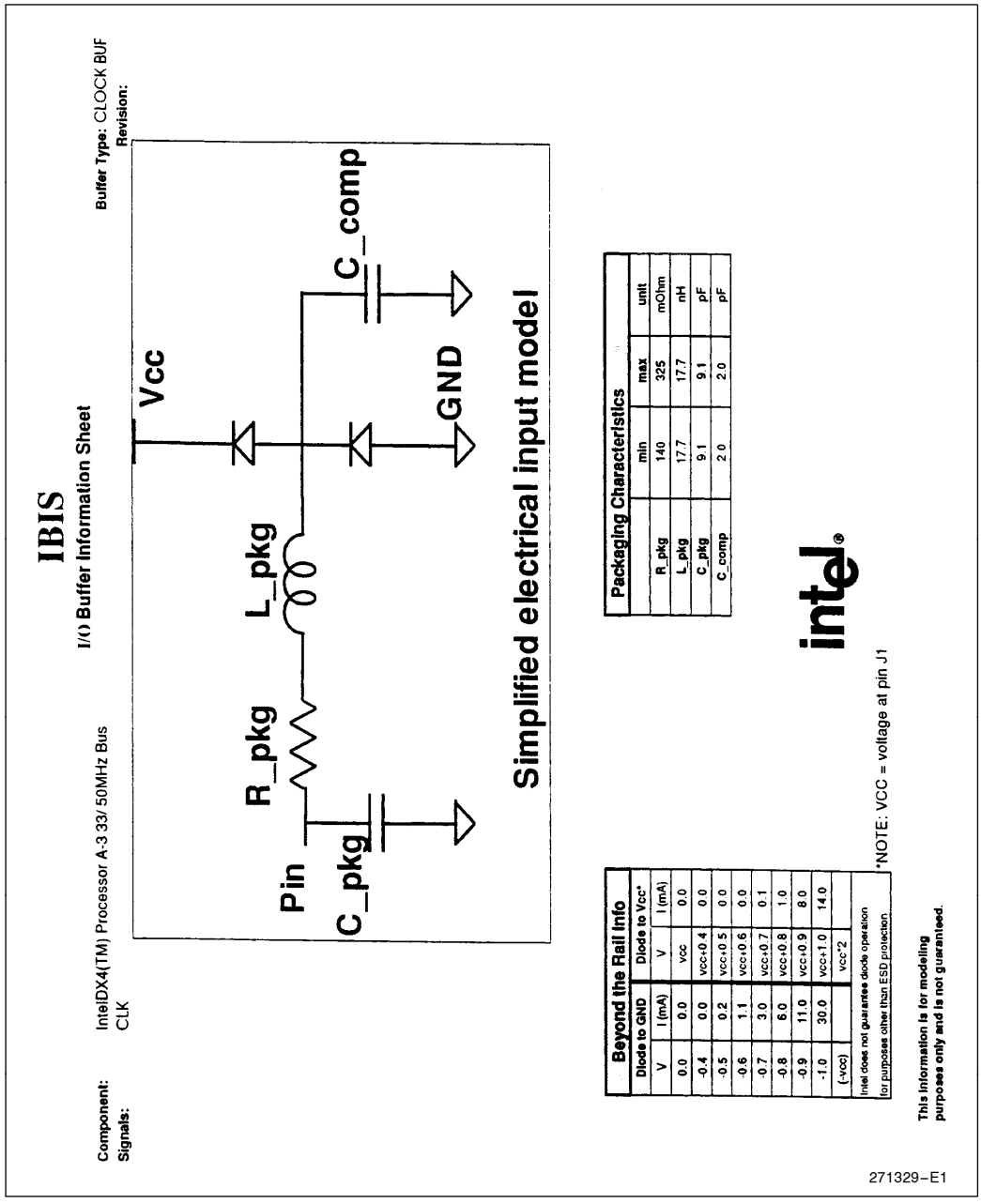
Each valid delay for the 50-MHz bus is specified for a 0 pF load. The system designer should use I/O buffer modeling to account for signal delays due to loading. Table B-1 lists the buffer type to be used for each signal in the external interface.

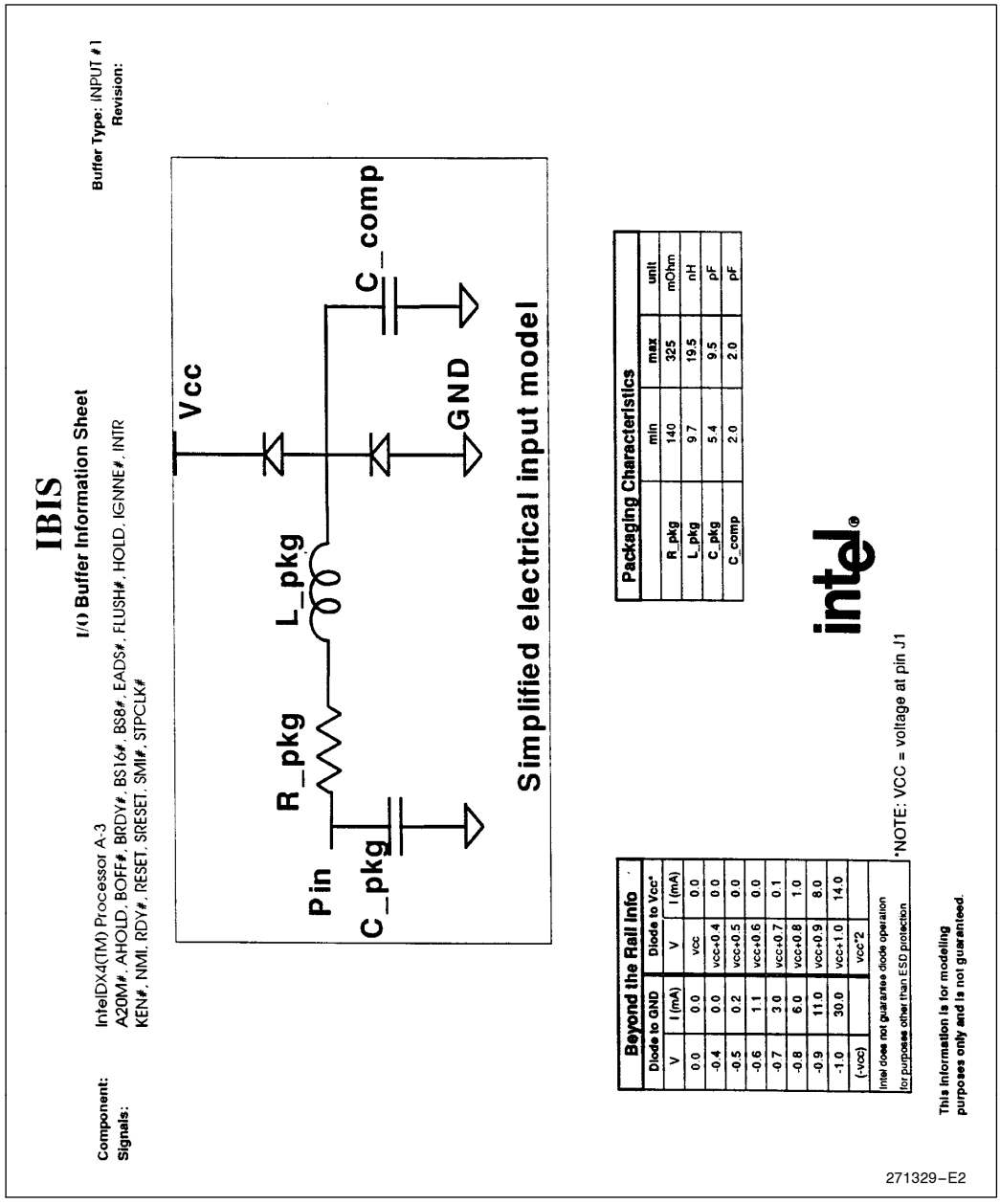
Table B-1. External Interface Signal Buffer Assignment

Device	Signals	Type	Drive Buffer TYPE	Receiver Buffer Type
IntelDX4™ Processor	A20M#, AHOLD, BOFF#, BRDY#, BS8# BS16#, FLUSH#, HOLD, IGNNE#, INTR, KEN#, NMI, RDY#, RESET#, EADS#, SMI#, STPCLK#, SRESET, CLKMUL	I	N/A	IN1
	CLK	I	N/A	CLK
	D16–D0, DP2–DP0	I/O	I/O1	IN1
	D31–D17, DP3	I/O	I/O2	IN1
	A31–A4	I/O	I/O3	IN1
	ADS#, BLAST#, LOCK#, PLOCK#, SMIACT#, A3–A2, FERR#, HLDA	O	O1	N/A
	BE3#–BE0#, BREQ#, D/C#, M/IO#, PCD, PWT, PCHK#, W/R#	O	O2	N/A

Sample IBIS Files for IntelDX4 Processor

The following pages present sample IBIS file outputs for the IntelDX4 processor.


IBIS
I/O Buffer Information Sheet
Component: IntelDX4(TM) Processor A-3 33/ 50MHz Bus
Signals: CLK
Buffer Type: CLOCK BUF
Revision:
Vcc
R_pkg
L_pkg
C_comp
Pin
C_pkg
GND
Simplified electrical input model
Beyond the Rail Info
Diode to GND
V | I (mA)
0.0 | 0.0
-0.4 | 0.0
-0.5 | 0.2
-0.6 | 1.1
-0.7 | 3.0
-0.8 | 6.0
-0.9 | 11.0
-1.0 | 30.0
(-vcc)
Diode to Vcc*
V | I (mA)
vcc | 0.0
vcc+0.4 | 0.0
vcc+0.5 | 0.0
vcc+0.6 | 0.0
vcc+0.7 | 0.1
vcc+0.8 | 1.0
vcc+0.9 | 8.0
vcc+1.0 | 14.0
vcc*2
Intel does not guarantee diode operation for purposes other than ESD protection
*NOTE: VCC = voltage at pin J1
Packaging Characteristics
min | max | unit
R_pkg | 140 | 325 | mOhm
L_pkg | 17.7 | 17.7 | nH
C_pkg | 9.1 | 9.1 | pF
C_comp | 2.0 | 2.0 | pF
This information is for modeling purposes only and is not guaranteed.
271329–E1

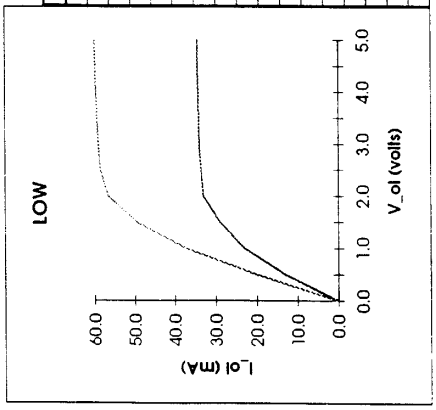

IBIS
I/O Buffer Information Sheet
Component: IntelDX4(TM) Processor A-3
Signals: A20M#, AHOLD, BOFF#, BRDY#, BS16#, BS8#, EADS#, FLUSH#, HOLD, IGNNE#, INTR
KEN#, NMI, RDY#, RESET, SRESET, SMI#, STPCLK#
Buffer Type: INPUT #1
Revision:
Vcc
R_pkg
L_pkg
C_comp
Pin
C_pkg
GND
Simplified electrical input model
Beyond the Rail Info
Diode to GND
V
I (mA)
Diode to Vcc*
V
I (mA)
0.0 0.0 vcc 0.0
-0.4 0.0 vcc+0.4 0.0
-0.5 0.2 vcc+0.5 0.0
-0.6 1.1 vcc+0.6 0.0
-0.7 3.0 vcc+0.7 0.1
-0.8 6.0 vcc+0.8 1.0
-0.9 11.0 vcc+0.9 8.0
-1.0 30.0 vcc+1.0 14.0
(-vcc) vcc*2
Intel does not guarantee diode operation for purposes other than ESD protection
*NOTE: VCC = voltage at pin J1
Packaging Characteristics
min max unit
R_pkg 140 325 mOhm
L_pkg 9.7 19.5 nH
C_pkg 5.4 9.5 pF
C_comp 2.0 2.0 pF
intel
This information is for modeling purposes only and is not guaranteed.
271329-E2

IBIS

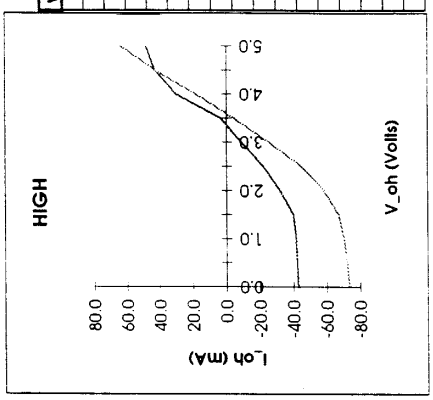
I/O Buffer Information Sheet

Component: IntelDX4(TM) Processor A-3 33/50MHz Bus
Signals: ADS#, BLAST#, SMIACT#, A<3:2>, FERR#, HLDA, PLOCK#, LOCK#

Buffer Type: OUT GROUP # 1
Revision:



V_ol	I_ol min	I_ol max	I_ol typ
-5.0	-1000	-1830	-1380
-2.0	-279.0	-472.0	-370.0
-1.0	-46.7	-57.1	-51.0
-0.5	-8.9	-20.7	-13.5
0.0	0.0	0.0	0.0
0.5	13.0	20.1	12.9
1.0	23.0	37.2	23.7
1.5	29.0	49.7	31.5
2.0	33.0	56.6	35.4
2.5	33.5	58.6	36.3
3.0	34.0	59.0	36.6
3.5	34.1	59.4	36.9
4.0	34.2	59.7	37.0
4.5	34.4	59.8	37.1
5.0	34.4	60.0	37.2
6.0	34.4	60.0	37.2
10.0	34.4	60.0	37.2



V_oh	I_oh min	I_oh max	I_oh typ
-5.0	-1050.0	-1880.0	-1410.0
-1.0	-66.7	-95.2	-79.8
0.0	-43.0	-73.5	-47.1
0.5	-42.0	-72.1	-46.1
1.0	-41.5	-70.2	-44.8
1.5	-40.0	-67.1	-42.1
2.0	-32.0	-58.5	-35.1
2.5	-22.0	-44.9	-24.1
3.0	-9.0	-25.2	-9.5
3.5	3.4	-4.6	6.5
4.0	30.0	18.1	24.3
4.5	43.0	43.0	41.7
5.0	48.5	64.0	56.4
5.5	55.4	80.9	67.3
6.0	59.3	93.4	74.6
7.0	62.2	104.0	79.8
10.0	63.7	109.0	82.4

Ramp Rate (into 0pF, no pkg)

	min	max	typ	unit
Rise	1.51	1.91	1.7	volts/ns
Fall	1.72	2.43	2.07	volts/ns

Simplified Output Resistance

	min	max	unit
Low	27.4	113.6	ohms
High	25.2	63.1	ohms

Simplified Output Resistance calculated using a 50 ohm load line

Beyond The Rail Info

Diode to GND		Diode to Vcc*	
V	I (mA)	V	I (mA)
0.0	0.0	vcc	0.0
-0.4	0.0	vcc+0.4	0.0
-0.5	0.2	vcc+0.5	0.0
-0.6	1.1	vcc+0.6	0.0
-0.7	3.0	vcc+0.7	0.1
-0.8	6.0	vcc+0.8	1.0
-0.9	11.0	vcc+0.9	8.0
-1.0	30.0	vcc+1.0	14.0
(-vcc)		vcc*2	

Intel does not guarantee diode operation for purposes other than ESD protection

Packaging Characteristics

	min	max	unit
R_pkg	140.0	325.0	mOhm
L_pkg	9.5	15.1	nH
C_pkg	5.6	9.7	pF
C_comp	2.9	3.2	pF

*NOTE: VCC = voltage at pin J1

This information is for modeling purposes only and is not guaranteed.

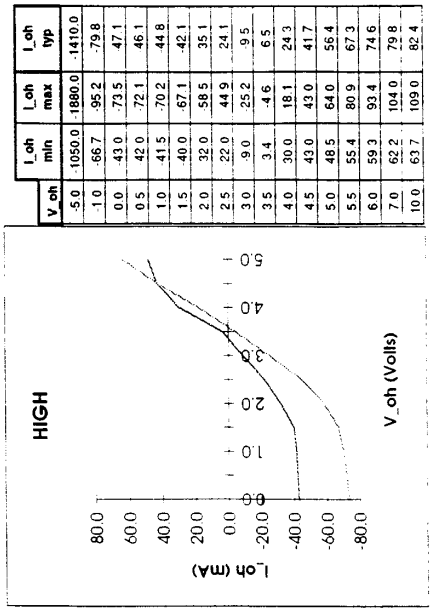
271329-E3

IBIS

I/O Buffer Information Sheet

Component: IntelDX4(TM) Processor A-3 33/ 50MHz Bus
Signals: BE<3:0>#, BREQ, D/C#, M/IO#, PWT, PCD, PCHK#, W/R#

Buffer Type: OUT GROUP #2
Revision:



V_ol	I_ol min	I_ol max	I_ol typ
5.0	-1000	-1830	-1380
2.0	279.0	472.0	370.0
1.0	46.7	57.1	51.0
0.5	8.9	20.7	13.5
0.0	0.0	0.0	0.0
0.5	13.0	20.1	12.9
1.0	23.0	37.2	23.7
1.5	29.0	49.7	31.5
2.0	33.0	56.6	35.4
2.5	33.5	58.6	36.3
3.0	34.0	59.0	36.6
3.5	34.1	59.4	36.9
4.0	34.2	59.7	37.0
4.5	34.4	59.8	37.1
5.0	34.4	60.0	37.2
6.0	34.4	60.0	37.2
10.0	34.4	60.0	37.2

V_oh	I_oh min	I_oh max	I_oh typ
5.0	-1050.0	-1880.0	-1410.0
1.0	-66.7	-95.2	-79.8
0.0	-43.0	-73.5	-47.1
0.5	-42.0	-72.1	-46.1
1.0	-41.5	-70.2	-44.8
1.5	-40.0	-67.1	-42.1
2.0	-32.0	-58.5	-35.1
2.5	-22.0	-44.9	-24.1
3.0	-9.0	-25.2	-9.5
3.5	3.4	-4.6	6.5
4.0	30.0	18.1	24.3
4.5	43.0	43.0	41.7
5.0	48.5	64.0	56.4
5.5	55.4	80.9	67.3
6.0	59.3	93.4	74.6
7.0	62.2	104.0	79.8
10.0	63.7	109.0	82.4

Ramp Rate (into 0pF, no pkg)

	min	max	typ	unit
Rise	1.51	1.91	1.7	volts/ns
Fall	1.72	2.43	2.07	volts/ns

Simplified Output Resistance

	min	max	unit
Low	27.4	113.6	ohms
High	25.2	63.1	ohms

Simplified Output Resistance calculated using a 50 ohm load line

Beyond The Rail Info

Diode to GND		Diode to Vcc*	
V	I (mA)	V	I (mA)
0.0	0.0	vcc	0.0
-0.4	0.0	vcc+0.4	0.0
-0.5	0.2	vcc+0.5	0.0
-0.6	1.1	vcc+0.6	0.0
-0.7	3.0	vcc+0.7	0.1
-0.8	6.0	vcc+0.8	1.0
-0.9	11.0	vcc+0.9	8.0
-1.0	30.0	vcc+1.0	14.0
(-vcc)		vcc*2	

Intel does not guarantee diode operation for purposes other than ESD protection

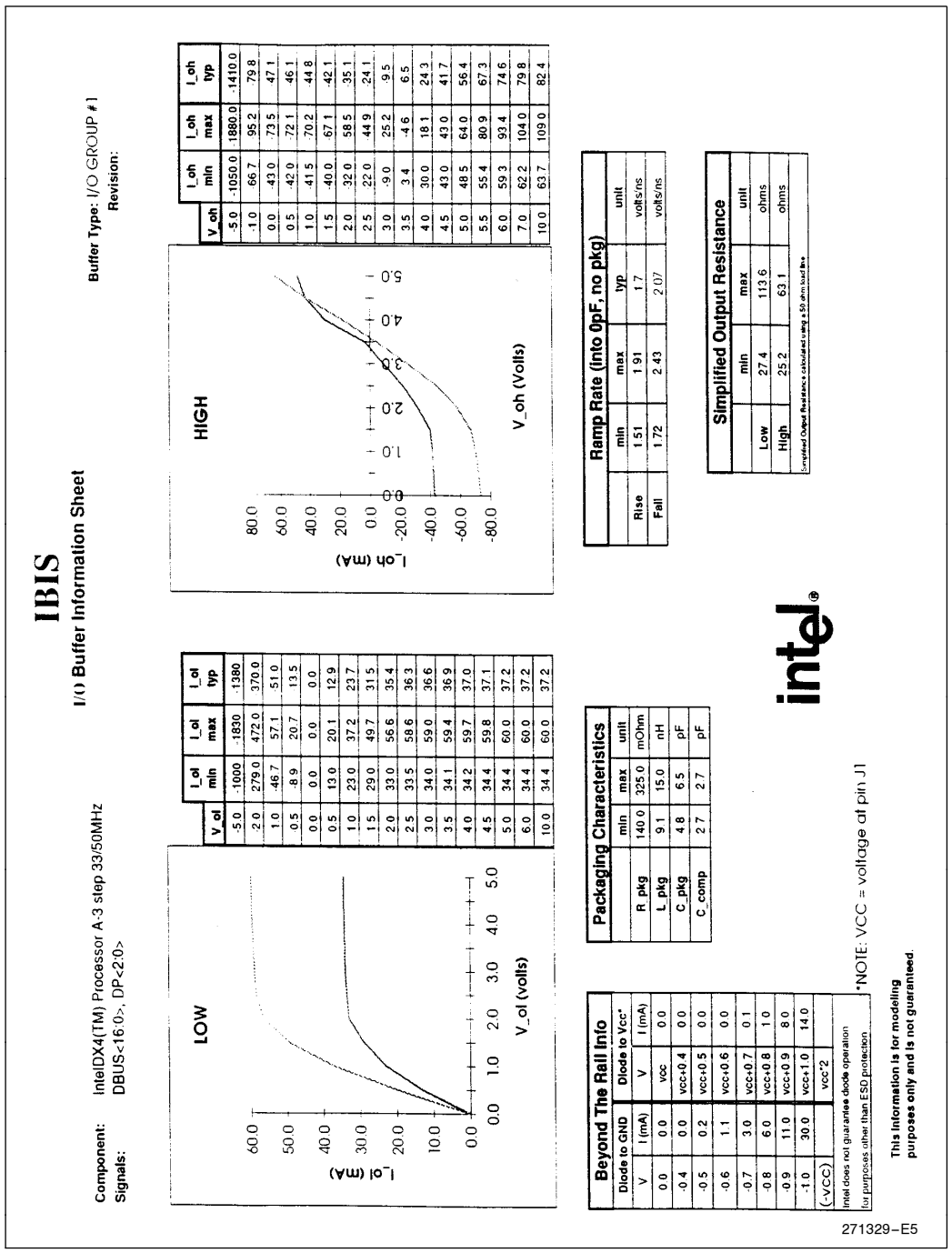
Packaging Characteristics

	min	max	unit
R_pkg	140	325	mOhm
L_pkg	8.5	20.4	nH
C_pkg	5.2	11.0	pF
C_comp	2.7	2.7	pF

*NOTE: VCC = voltage at pin J1

This information is for modeling purposes only and is not guaranteed.

271329–E4



IBIS

I/O Buffer Information Sheet

Component: IntelDX4(TM) Processor A-3 step 33/50MHz

Signals: DBUS<16:0>, DP<2:0>

Buffer Type: I/O GROUP #1

Revision:

LOW

V_ol	I_ol min	I_ol max	I_ol typ
-5.0	-1000	-1830	-1380
-2.0	-279.0	-472.0	-370.0
-1.0	-46.7	-57.1	-51.0
-0.5	-8.9	-20.7	-13.5
0.0	0.0	0.0	0.0
0.5	13.0	20.1	12.9
1.0	23.0	37.2	23.7
1.5	29.0	49.7	31.5
2.0	33.0	56.6	35.4
2.5	33.5	58.6	36.3
3.0	34.0	59.0	36.6
3.5	34.1	59.4	36.9
4.0	34.2	59.7	37.0
4.5	34.4	59.8	37.1
5.0	34.4	60.0	37.2
6.0	34.4	60.0	37.2
10.0	34.4	60.0	37.2

HIGH

V_oh	I_oh min	I_oh max	I_oh typ
-5.0	-1050.0	-1880.0	-1410.0
-1.0	-66.7	-95.2	-79.8
0.0	-43.0	-73.5	-47.1
0.5	-42.0	-72.1	-46.1
1.0	-41.5	-70.2	-44.8
1.5	-40.0	-67.1	-42.1
2.0	-32.0	-58.5	-35.1
2.5	-22.0	-44.9	-24.1
3.0	-9.0	-25.2	-9.5
3.5	3.4	-4.6	6.5
4.0	30.0	18.1	24.3
4.5	43.0	43.0	41.7
5.0	48.5	64.0	56.4
5.5	55.4	80.9	67.3
6.0	59.3	93.4	74.6
7.0	62.2	104.0	79.8
10.0	63.7	109.0	82.4

Ramp Rate (into 0pF, no pkg)

	min	max	typ	unit
Rise	1.51	1.91	1.7	volts/ns
Fall	1.72	2.43	2.07	volts/ns

Simplified Output Resistance

	min	max	unit
Low	27.4	113.6	ohms
High	25.2	63.1	ohms

Simplified Output Resistance calculated using ±50 ohm load line

Beyond The Rail Info

Diode to GND		Diode to Vcc*	
V	I (mA)	V	I (mA)
0.0	0.0	vcc	0.0
-0.4	0.0	vcc+0.4	0.0
-0.5	0.2	vcc+0.5	0.0
-0.6	1.1	vcc+0.6	0.0
-0.7	3.0	vcc+0.7	0.1
-0.8	6.0	vcc+0.8	1.0
-0.9	11.0	vcc+0.9	8.0
-1.0	30.0	vcc+1.0	14.0
(-VCC)		vcc*2	

Intel does not guarantee diode operation for purposes other than ESD protection.

Packaging Characteristics

	min	max	unit
R_pkg	140.0	325.0	mOhm
L_pkg	9.1	15.0	nH
C_pkg	4.8	6.5	pF
C_comp	2.7	2.7	pF

*NOTE: VCC = voltage at pin J1

This information is for modeling purposes only and is not guaranteed.

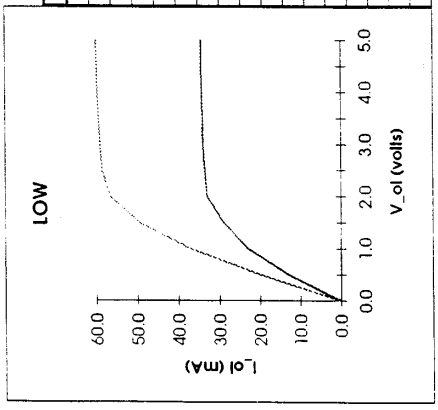
271329–E5

IBIS

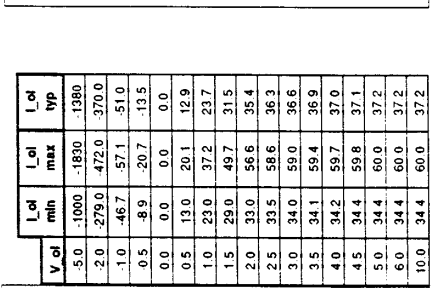
I/O Buffer Information Sheet

Component: IntelDX4(TM) Processor A 3 33/ 50MHz Bus
Signals: DBUS<31:17>, DP<3>

Buffer Type: I/O GROUP # 1
Revision:



V_ol	I_ol min	I_ol max	I_ol typ
-5.0	-1000	-1830	-1380
-2.0	-279.0	-472.0	-370.0
-1.0	-46.7	-57.1	-51.0
0.5	-8.9	-20.7	-13.5
0.0	0.0	0.0	0.0
0.5	13.0	20.1	12.9
1.0	23.0	37.2	23.7
1.5	29.0	49.7	31.5
2.0	33.0	56.6	35.4
2.5	33.5	58.6	36.3
3.0	34.0	59.0	36.6
3.5	34.1	59.4	36.9
4.0	34.2	59.7	37.0
4.5	34.4	59.8	37.1
5.0	34.4	60.0	37.2
6.0	34.4	60.0	37.2
10.0	34.4	60.0	37.2



V_oh	I_oh min	I_oh max	I_oh typ
5.0	-1050.0	-1880.0	-1410.0
1.0	-66.7	-95.2	-79.8
0.0	-43.0	-73.5	-47.1
0.5	-42.0	-72.1	-46.1
1.0	-41.5	-70.2	-44.8
1.5	-40.0	-67.1	-42.1
2.0	-32.0	-58.5	-35.1
2.5	-22.0	-44.9	-24.1
3.0	-9.0	-25.2	-9.5
3.5	3.4	-4.6	6.5
4.0	30.0	18.1	24.3
4.5	43.0	43.0	41.7
5.0	48.5	64.0	56.4
5.5	55.4	80.9	67.3
6.0	59.3	93.4	74.6
7.0	62.2	104.0	79.8
11.0	63.7	109.0	82.4

Ramp Rate (into 0pF, no pkg)

	min	max	typ	unit
Rise	1.51	1.91	1.7	volts/ns
Fall	1.72	2.43	2.07	volts/ns

Simplified Output Resistance

	min	max	unit
Low	27.4	113.6	ohms
High	25.2	63.1	ohms

Simplified Output Resistance calculated using a 50 ohm load line

Packaging Characteristics

	min	max	unit
R_pkg	140.0	325.0	mOhm
L_pkg	8.5	13.7	nH
C_pkg	4.0	6.3	pF
C_comp	2.9	3.2	pF

Beyond The Rail Info

Diode to GND		Diode to Vcc*	
V	I (mA)	V	I (mA)
0.0	0.0	vcc	0.0
-0.4	0.0	vcc+0.4	0.0
-0.5	0.2	vcc+0.5	0.0
-0.6	1.1	vcc+0.6	0.0
-0.7	3.0	vcc+0.7	0.1
-0.8	6.0	vcc+0.8	1.0
-0.9	11.0	vcc+0.9	8.0
-1.0	30.0	vcc+1.0	14.0
(-vcc)		vcc*2	

Intel does not guarantee diode operation for purposes other than ESD protection

*NOTE: VCC = voltage at pin J1

This information is for modeling purposes only and is not guaranteed.

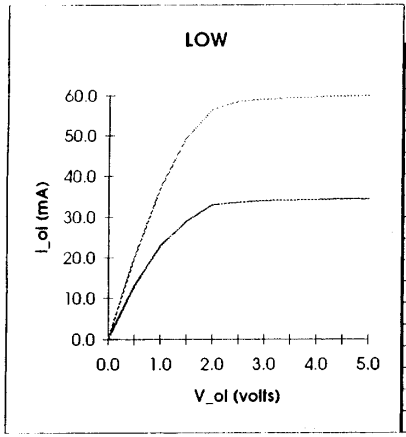
271329-E6

IBIS

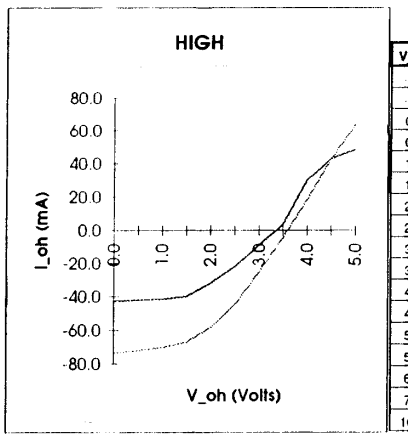
I/O Buffer Information Sheet

Component: IntelDX4(TM) Processor A-3 33/ 50MHz Bus
Signals: ABUS<31:4>

Buffer Type: I/O GROUP #3
Revision:



V_ol	I_ol min	I_ol max	I_ol typ
5.0	-1000	-1830	-1380
2.0	-279.0	-472.0	-370.0
1.0	-46.7	-57.1	-51.0
0.5	-8.9	-20.7	-13.5
0.0	0.0	0.0	0.0
0.5	13.0	20.1	12.9
1.0	23.0	37.2	23.7
1.5	29.0	49.7	31.5
2.0	33.0	56.6	35.4
2.5	33.5	58.6	36.3
3.0	34.0	59.0	36.6
3.5	34.1	59.4	36.9
4.0	34.2	59.7	37.0
4.5	34.4	59.8	37.1
5.0	34.4	60.0	37.2
6.0	34.4	60.0	37.2
10.0	34.4	60.0	37.2



V_oh	I_oh min	I_oh max	I_oh typ
5.0	-1050.0	1880.0	-1410.0
1.0	-66.7	-95.2	-79.8
0.0	-43.0	-73.5	-47.1
0.5	-42.0	-72.1	-46.1
1.0	-41.5	-70.2	-44.8
1.5	-40.0	-67.1	-42.1
2.0	-32.0	-58.5	-35.1
2.5	-22.0	-44.9	-24.1
3.0	-9.0	-25.2	-9.5
3.5	3.4	-4.6	6.5
4.0	30.0	18.1	24.3
4.5	43.0	43.0	41.7
5.0	48.5	64.0	56.4
5.5	55.4	80.9	67.3
6.0	59.3	93.4	74.6
7.0	62.2	104.0	79.8
10.0	63.7	109.0	82.4

Beyond The Rail Info

Diode to GND		Diode to Vcc*	
V	I (mA)	V	I (mA)
0.0	0.0	vcc	0.0
0.4	0.0	vcc+0.4	0.0
0.5	0.2	vcc+0.5	0.0
0.6	1.1	vcc+0.6	0.0
0.7	3.0	vcc+0.7	0.1
0.8	6.0	vcc+0.8	1.0
0.9	11.0	vcc+0.9	8.0
1.0	30.0	vcc+1.0	14.0
(-VCC)		vcc*2	

Intel does not guarantee diode operation for purposes other than ESD protection

Packaging Characteristics

	min	max	unit
R_pkg	140	325	mOhm
L_pkg	7.9	14.7	nH
C_pkg	4.4	7.4	pF
C_comp	2.9	2.9	pF

Ramp Rate (into 0pF, no pkg)

	min	max	typ	unit
Rise	1.51	1.91	1.7	volts/ns
Fall	1.72	2.43	2.07	volts/ns

Simplified Output Resistance

	min	max	unit
Low	27.4	113.6	ohms
High	25.2	63.1	ohms

Simplified Output Resistance calculated using a 50 ohm load line

*NOTE: VCC = voltage at pin J1

271329-E7

This information is for modeling purposes only and is not guaranteed.

Sample Text Listing of IBIS Files for IntelDX4 Processor

```
|**************************************************************************
|
[IBIS Ver]     1.1
[File name]    inteldx4pg.ibs
[File Rev]     2.0
[Date]         3/23/94
[Source]       File originated at Intel Corporation
[Notes]        The following information corresponds to the INTELDX4(TM)
|              processor and has been correlated with silicon.  This file
               is for the PGA package only.IntelDX4 processor
[Disclaimer]   This information is for modeling purposes only, and is not
|              guaranteed.
|
|**************************************************************************
|
|
[Component]      INTELDX4 PROCESSOR
[Manufacturer]   Intel
[Package]
|
|     typ   min         max
R_pkg       2329m 728m  3930m
L_pkg       17.79nH     8.56nH      27.01nH
C_pkg       6.03pF      1.89pF      10.16pF
|
|
|**************************************************************************
|
[Pin]    signal_name      model_name   R_pin    L_pin    C_pin
 A01     D20                 I/O2         1866m    15.54n    3.88p
 A02     D22                 I/O2         1808m    13.70n    5.60p
 A04     D23                 I/O2         1468m    13.33n    3.14p
 A05     DP3                 I/O2         1406m    11.59n    4.50p
 A06     D24                 I/O2         1412m    13.02n    3.04p
 A08     D29                 I/O2         1274m    10.90n    4.14p
 A15     IGNNE#              Input1       1858m    13.96n    5.74p
 A16     INTR                Input1       1956m    14.47n    6.00p
 A17     AHOLD               Input1       3414m    22.11n    9.99p
 B01     D19                 I/O2         1762m    13.46n    5.47p
 B02     D21                 I/O2         1636m    14.27n    3.45p
 B06     D25                 I/O2         1178m    11.72n    2.61p
 B08     D31                 I/O2         1050m     9.73n    3.52p
 B10     SMI#                Input1       948m     10.45n    2.19p
 B15     NMI                 Input1       1430m    13.12n    3.07p
 B17     EADS#               Input1       1728m    14.78n    3.62p
 C01     D11                 I/O1         2440m    18.73n    4.93p
 C02     D18                 I/O2         1446m    13.21n    3.10p
 C03     CLK                 Clockbuffer  2486m    18.99n    5.02p
 C06     D27                 I/O2         964m     10.54n    2.21p
 C07     D26                 I/O2         892m     8.90n     3.09p
 C08     D28                 I/O2         752m     9.36n     1.82p
 C09     D30                 I/O2         728m     9.22n     1.78p
 C10     SRESET              Input1       784m     9.54n     1.88p
 C12     SMIACT#             Output1      1270m    12.23n    2.78p
```

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C14	FERR#	Output1	1904m	15.76n	3.95p
C15	FLUSH#	Input1	1342m	11.26n	4.32p
C16	RESET	Input1	1480m	11.98n	4.70p
C17	BS16#	Input1	2756m	20.49n	5.52p
D01	D9	I/O1	2718m	18.47n	8.09p
D02	D13	I/O1	2100m	16.84n	4.31p
D03	D17	I/O2	1156m	11.60n	2.57p
D15	A20M#	Input1	1148m	11.56n	2.55p
D16	BS8#	Input1	3474m	22.43n	10.16p
D17	BOFF#	Input1	3452m	22.31n	10.10p
E03	D10	I/O1	2356m	16.57n	7.10p
E15	HOLD	Input1	1920m	15.85n	3.98p
F01	DP1	I/O1	2394m	16.77n	7.20p
F02	D8	I/O1	1864m	15.53n	3.87p
F03	D15	I/O1	858m	9.95n	2.02p
F15	KEN#	Input1	2404m	16.82n	7.23p
F16	RDY#	Input1	1804m	15.20n	3.76p
F17	BE3#	Output2	3336m	23.71n	6.58p
G03	D12	I/O1	1912m	14.24n	5.88p
G15	STPCLK#	Input1	3930m	27.01n	7.68p
H02	D3	I/O1	1708m	14.67n	3.59p
H03	DP2	I/O1	928m	9.09n	3.19p
H15	BRDY#	Input1	2134m	17.03n	4.37p
J02	D5	I/O1	1528m	13.67n	3.25p
J03	D16	I/O1	1614m	14.14n	3.41p
J15	BE2#	Output2	848m	8.67n	2.97p
J16	BE1#	Output2	1002m	10.75n	2.28p
J17	PCD	Output2	2266m	17.77n	4.61p
K03	D14	I/O1	1160m	10.30n	3.83p
K15	BE0#	Output2	954m	9.22n	3.26p
L02	D6	I/O1	1432m	11.73n	4.57p
L03	D7	I/O1	1048m	11.00n	2.37p
L15	PWT	Output2	1548m	12.34n	4.89p
M03	D4	I/O1	1000m	9.47n	3.39p
M15	D/C#	Output2	1442m	13.19n	3.10p
N01	D2	I/O1	1448m	11.81n	4.61p
N02	D1	I/O1	1198m	11.84n	2.65p
N03	DP0	I/O1	1038m	10.95n	2.35p
N15	LOCK#	Output1	1118m	10.09n	3.71p
N16	M/IO#	Output2	1744m	14.87n	3.65p
N17	W/R#	Output2	1676m	13.01n	5.24p
P01	D0	I/O1	1532m	12.25n	4.84p
P02	A29	I/O3	1292m	12.36n	2.82p
P03	A30	I/O3	1194m	10.48n	3.92p
P15	HLDA	Output1	1568m	13.89n	3.33p
Q01	A31	I/O3	1608m	14.11n	3.40p
Q03	A17	I/O3	2016m	16.38n	4.15p
Q04	A19	I/O3	1584m	12.53n	4.99p
Q05	A21	I/O3	956m	10.49n	2.20p
Q06	A24	I/O3	920m	9.05n	3.17p
Q07	A22	I/O3	894m	8.91n	3.10p
Q08	A20	I/O3	788m	9.56n	1.89p
Q09	A16	I/O3	850m	8.68n	2.98p
Q10	A13	I/O3	836m	9.82n	1.98p
Q11	A9	I/O3	914m	9.02n	3.15p
Q12	A5	I/O3	966m	9.29n	3.29p

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```
 Q13    A7                  I/O3         1084m   11.20n   2.44p
 Q14    A2                  Output1      1134m   11.48n   2.53p
 Q15    BREQ                Output2      1872m   15.58n   3.89p
 Q16    PLOCK#              Output1      1630m   14.23n   3.44p
 Q17    PCHK#               Output2      1616m   12.69n   5.07p
 R01    A28                 I/O3         1708m   14.67n   3.59p
 R02    A25                 I/O3         1604m   12.63n   5.04p
 R05    A18                 I/O3         1498m   13.50n   3.20p
 R07    A15                 I/O3         1148m   11.56n   2.55p
 R12    A11                 I/O3         1274m   10.90n   4.14p
 R13    A8                  I/O3         1252m   12.13n   2.75p
 R15    A3                  Output1      1504m   12.11n   4.77p
 R16    BLAST#              Output1      1698m   14.61n   3.57p
 S01    A27                 I/O3         1900m   14.18n   5.85p
 S02    A26                 I/O3         1800m   15.18n   3.75p
 S03    A23                 I/O3         1756m   14.93n   3.67p
 S05    A14                 I/O3         1842m   13.88n   5.69p
 S07    A12                 I/O3         1530m   12.24n   4.84p
 S13    A10                 I/O3         1444m   13.20n   3.10p
 S15    A6                  I/O3         1722m   13.25n   5.36p
 S16    A4                  I/O3         1792m   15.13n   3.74p
 S17    ADS#                Output1      1888m   14.12n   5.82p
|
|*******************************************************************************
|
[Model]  Output1
Model_type Output
Polarity Non-Inverting
Enable  Active-Low
|signals ADS#,BLAST#,SMIACT#,A<3:2>,FERR#,HLDA,PLOCK#,LOCK#
|
|          typ   min   max
C_comp     3.05pF  2.9pF   3.2pF
[Voltage range] 3.3V  3.0V  3.6V
|
|*******************************************************************************
|
[Pulldown]
| voltage  I(typ)    I(min)    I(max)
 -5.0V   -960.0mA  -580.0mA  -1410mA
 -2.0V   -190.0mA  -99.0mA  -292.0mA
 -1.0V   -21.0mA  -16.7mA  -27.1mA
 -0.5V   -13.30mA  -8.7mA   -20.5mA
 0.0V   0.0   0.0   0.0
 0.5V   12.9mA   8.3mA   20.1mA
 1.0V   23.7mA   15.1mA   37.2mA
 1.5V   31.5mA   19.7mA   49.7mA
 2.0V   35.4mA   21.6mA   56.6mA
 2.5V   36.3mA   22.0mA   58.6mA
 3.0V   36.6mA   22.2mA   59.0mA
 3.5V   36.9mA   22.3mA   59.4mA
 4.0V   37.0mA   22.4mA   59.7mA
 4.5V   37.1mA   22.5mA   59.8mA
 5.0V   37.2mA   22.5mA   60.0mA
 6.0V   37.2mA   22.5mA   60.0mA
 10.0V   37.2mA   22.5mA   60.0mA
```

271329-F0

```
|
|*************************************************************************
| Note that the pullup voltage in the data table is derived from
| the equation:
|  Vtable = Vcc - Voutput
| For the 8.3V in the table, it is actually 8.3V below Vcc and -5V
| with respected to Ground.
|*************************************************************************
|
[Pullup]
| voltage  I(typ)  I(min)  I(max)
|
 8.3V   -1410mA  -976.25mA -1992.8mA
 4.3V  -79.8mA  -55.6mA  -229.06mA
 3.3V   -47.1mA  -40.80mA -72.66mA
 2.8V   -46.1mA  -29.42mA -70.96mA
 2.3V   -44.8mA  -28.64mA -68.34mA
 1.8V   -42.1mA  -27.14mA -61.94mA
 1.3V   -35.1mA  -23.34mA -50.34mA
 0.8V  -24.1mA  -16.08mA -33.08mA
 0.3V   -9.5mA   -6.3mA  -12.86mA
 -0.2V   6.5mA   4.76mA  9.02mA
 -0.7V   24.3mA   17.3mA  33.04mA
 -1.2V   41.7mA   30.48mA  55.6mA
 -1.7V   56.4mA   42.26mA  74.14mA
 -2.2V   67.3mA   51.26mA  88.4mA
 -2.7V   74.6mA   56.96mA  96.58mA
 -3.7V   79.8mA   61.33mA  104.5mA
 -6.7V   82.4mA   63.55mA  109.5mA
|
[GND_clamp]
| Voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  -0.2mA  NA  NA
 -0.6V  -1.1mA  NA  NA
 -0.7V  -3.0mA  NA  NA
 -0.8V  -6.0mA  NA  NA
 -0.9V  -11.0mA  NA  NA
 -1.0V  -30.0mA  NA  NA
 -1.2V  -120.0mA NA  NA
 -2.0V  -180.0mA NA  NA
 -5.0V  -420.0mA NA  NA
|
|*************************************************************************
|  The data in the following POWER_clamp table is listed
| as "Vcc-relative", meaning that the voltage values are
| referenced to the Vcc pin.  The voltages in the data tables
|  are derived from the equation:
|   Vtable = Vcc - Voutput
| In this case, assuming that Vcc  is referenced to 3.3V.
| 0V in the table actually means 3.3V with respected to
| Ground and 0V above Vcc.
|*************************************************************************
|
[POWER_clamp]
```

271329-F1

```
| voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  0mA  NA  NA
 -0.6V  0mA  NA  NA
 -0.7V  0.1mA  NA  NA
 -0.8V  1.0mA  NA  NA
 -0.9V  8.0mA  NA  NA
 -1.0V  14.0mA  NA  NA
 -2.0V  100mA  NA  NA
|
|*****************************************************************************
|
[Ramp]
|  typ  min  max
dV/dt_r  1.13/0.749n 0.93/0.868n 1.35/0.642n
dV/dt_f  0.99/0.447n 0.75/0.543n 1.27/0.387n
|
|*****************************************************************************
|
[Model]  Output2
Model_type Output
Polarity Non-Inverting
Enable  Active-Low
|signal  BE<3:0>#,BREQ,D/C#,M/IO#,PWT,PCD,PCHK#,W/R#
|
|          typ   min   max
C_comp     2.7pF      2.7pF      2.7pF
[Voltage range] 3.3V  3.0V  3.6V
|
|*****************************************************************************
|
[Pulldown]
| voltage  I(typ)  I(min)  I(max)
 -5.0V   -960.0mA  -580.0mA  -1410mA
 -2.0V   -190.0mA  -99.0mA  -292.0mA
 -1.0V   -21.0mA  -16.7mA  -27.1mA
 -0.5V   -13.30mA  -8.7mA   -20.5mA
 0.0V   0.0   0.0   0.0
 0.5V   12.9mA   8.3mA   20.1mA
 1.0V   23.7mA   15.1mA   37.2mA
 1.5V   31.5mA   19.7mA   49.7mA
 2.0V   35.4mA   21.6mA   56.6mA
 2.5V   36.3mA   22.0mA   58.6mA
 3.0V   36.6mA   22.2mA   59.0mA
 3.5V   36.9mA   22.3mA   59.4mA
 4.0V   37.0mA   22.4mA   59.7mA
 4.5V   37.1mA   22.5mA   59.8mA
 5.0V   37.2mA   22.5mA   60.0mA
 6.0V   37.2mA   22.5mA   60.0mA
 10.0V   37.2mA   22.5mA   60.0mA
|
|*****************************************************************
| Note that the pullup voltage in the data table is derived from
| the equation:
|  Vtable = Vcc - Voutput
```

271329-F2

```
| For the 8.3V in the table, it is actually 8.3V below Vcc and -5V
| with respected to Ground.
|*****************************************************************
|
[Pullup]
| Voltage  I(typ)  I(min)  I(max)
|
 8.3V   -1410mA  -976.25mA -1992.8mA
 4.3V  -79.8mA  -55.6mA  -229.06mA
 3.3V   -47.1mA  -40.80mA -72.66mA
 2.8V   -46.1mA  -29.42mA -70.96mA
 2.3V   -44.8mA  -28.64mA -68.34mA
 1.8V   -42.1mA  -27.14mA -61.94mA
 1.3V   -35.1mA  -23.34mA -50.34mA
 0.8V  -24.1mA  -16.08mA -33.08mA
 0.3V   -9.5mA   -6.3mA  -12.86mA
 -0.2V   6.5mA   4.76mA  9.02mA
 -0.7V   24.3mA   17.3mA  33.04mA
 -1.2V   41.7mA   30.48mA  55.6mA
 -1.7V   56.4mA   42.26mA  74.14mA
 -2.2V   67.3mA   51.26mA  88.4mA
 -2.7V   74.6mA   56.96mA  96.58mA
 -3.7V   79.8mA   61.33mA  104.5mA
 -6.7V   82.4mA   63.55mA  109.5mA
|
[GND_clamp]
|
| Voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  -0.2mA  NA  NA
 -0.6V  -1.1mA  NA  NA
 -0.7V  -3.0mA  NA  NA
 -0.8V  -6.0mA  NA  NA
 -0.9V  -11.0mA  NA  NA
 -1.0V  -30.0mA  NA  NA
 -1.2V  -120.0mA NA  NA
 -2.0V  -180.0mA NA  NA
 -5.0V  -420.0mA NA  NA
|
|*********************************************************************
|  The data in the following POWER_clamp table is listed
| as "Vcc-relative", meaning that the voltage values are
| referenced to the Vcc pin.  The voltages in the data tables
|  are derived from the equation:
|   Vtable = Vcc - Voutput
| In this case, assuming that Vcc  is referenced to 3.3V.
| 0V in the table actually means 3.3V with respected to
| Ground and 0V above Vcc.
|*********************************************************************
|
[POWER_clamp]
| voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  0mA  NA  NA
```

271329-F3

```
 -0.6V  0mA  NA  NA
 -0.7V  0.1mA  NA  NA
 -0.8V  1.0mA  NA  NA
 -0.9V  8.0mA  NA  NA
 -1.0V  14.0mA  NA  NA
 -2.0V  100mA  NA  NA
|
[Ramp]
|  typ  min  max
dV/dt_r  1.13/0.749n 0.93/0.868n 1.35/0.642n
dV/dt_f  0.99/0.447n 0.75/0.543n 1.27/0.387n
|
|*********************************************************************
|
[Model]  I/O1
Model_type I/O
Polarity Non-Inverting
Enable  Active-Low
Vinl = 0.8v
Vinh = 2.0v
|signal  DBUS<16:0>,DP<2:0>
|
|          typ   min   max
C_comp     2.7pF      2.7pF      2.7pF
[Voltage range] 3.3V  3.0V  3.6V
|
|*********************************************************************
|
[Pulldown]
| voltage  I(typ)  I(min)  I(max)
 -5.0V   -960.0mA  -580.0mA  -1410mA
 -2.0V   -190.0mA  -99.0mA  -292.0mA
 -1.0V   -21.0mA  -16.7mA  -27.1mA
 -0.5V   -13.30mA  -8.7mA   -20.5mA
 0.0V   0.0   0.0   0.0
 0.5V   12.9mA   8.3mA   20.1mA
 1.0V   23.7mA   15.1mA   37.2mA
 1.5V   31.5mA   19.7mA   49.7mA
 2.0V   35.4mA   21.6mA   56.6mA
 2.5V   36.3mA   22.0mA   58.6mA
 3.0V   36.6mA   22.2mA   59.0mA
 3.5V   36.9mA   22.3mA   59.4mA
 4.0V   37.0mA   22.4mA   59.7mA
 4.5V   37.1mA   22.5mA   59.8mA
 5.0V   37.2mA   22.5mA   60.0mA
 6.0V   37.2mA   22.5mA   60.0mA
 10.0V   37.2mA   22.5mA   60.0mA
|
|*****************************************************************
| Note that the pullup voltage in the data table is derived from
| the equation:
|  Vtable = Vcc - Voutput
| For the 8.3V in the table, it is actually 8.3V below Vcc and -5V
| with respected to Ground.
|*****************************************************************
|
```

271329-F4

```
[Pullup]
| voltage  I(typ)  I(min)  I(max)
|
 8.3V   -1410mA  -976.25mA -1992.8mA
 4.3V  -79.8mA  -55.6mA  -229.06mA
 3.3V   -47.1mA  -40.80mA -72.66mA
 2.8V   -46.1mA  -29.42mA -70.96mA
 2.3V   -44.8mA  -28.64mA -68.34mA
 1.8V   -42.1mA  -27.14mA -61.94mA
 1.3V   -35.1mA  -23.34mA -50.34mA
 0.8V  -24.1mA  -16.08mA -33.08mA
 0.3V   -9.5mA   -6.3mA  -12.86mA
 -0.2V   6.5mA   4.76mA  9.02mA
 -0.7V   24.3mA   17.3mA  33.04mA
 -1.2V   41.7mA   30.48mA  55.6mA
 -1.7V   56.4mA   42.26mA  74.14mA
 -2.2V   67.3mA   51.26mA  88.4mA
 -2.7V   74.6mA   56.96mA  96.58mA
 -3.7V   79.8mA   61.33mA  104.5mA
 -6.7V   82.4mA   63.55mA  109.5mA
|
[GND_clamp]
| Voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  -0.2mA  NA  NA
 -0.6V  -1.1mA  NA  NA
 -0.7V  -3.0mA  NA  NA
 -0.8V  -6.0mA  NA  NA
 -0.9V  -11.0mA  NA  NA
 -1.0V  -30.0mA  NA  NA
 -1.2V  -120.0mA NA  NA
 -2.0V  -180.0mA NA  NA
 -5.0V  -420.0mA NA  NA
|
|*********************************************************************
|  The data in the following POWER_clamp table is listed
| as "Vcc-relative", meaning that the voltage values are
| referenced to the Vcc pin.  The voltages in the data tables
|  are derived from the equation:
|   Vtable = Vcc - Voutput
| In this case, assuming that Vcc  is referenced to 3.3V.
| 0V in the table actually means 3.3V with respected to
| Ground and 0V above Vcc.
|*********************************************************************
|
[POWER_clamp]
| voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  0mA  NA  NA
 -0.6V  0mA  NA  NA
 -0.7V  0.1mA  NA  NA
 -0.8V  1.0mA  NA  NA
 -0.9V  8.0mA  NA  NA
 -1.0V  14.0mA  NA  NA
```

271329-F5

```
 -2.0V  100mA  NA  NA
|
[Ramp]
|  typ  min  max
dV/dt_r  1.13/0.749n 0.93/0.868n 1.35/0.642n
dV/dt_f  0.99/0.447n 0.75/0.543n 1.27/0.387n
|
|*********************************************************************
|
[Model]  I/O2
Model_type I/O
Polarity Non-Inverting
Enable  Active-Low
Vinl = 3.3v
Vinh = 6.0v
|siganl  DBUS<31:17>,DP<3>
|
|  typ  min  max
C_comp  3.05pF  2.9pF  3.2pF
[Voltage range]  3.3V 3.0V 3.6V
|
|*********************************************************************
|
[Pulldown]
| voltage  I(typ)  I(min)  I(max)
 -5.0V   -960.0mA  -580.0mA  -1410mA
 -2.0V   -190.0mA  -99.0mA  -292.0mA
 -1.0V   -21.0mA  -16.7mA  -27.1mA
 -0.5V   -13.30mA  -8.7mA   -20.5mA
 0.0V   0.0   0.0   0.0
 0.5V   12.9mA   8.3mA   20.1mA
 1.0V   23.7mA   15.1mA   37.2mA
 1.5V   31.5mA   19.7mA   49.7mA
 2.0V   35.4mA   21.6mA   56.6mA
 2.5V   36.3mA   22.0mA   58.6mA
 3.0V   36.6mA   22.2mA   59.0mA
 3.5V   36.9mA   22.3mA   59.4mA
 4.0V   37.0mA   22.4mA   59.7mA
 4.5V   37.1mA   22.5mA   59.8mA
 5.0V   37.2mA   22.5mA   60.0mA
 6.0V   37.2mA   22.5mA   60.0mA
 10.0V   37.2mA   22.5mA   60.0mA
|
|*****************************************************************
| Note that the pullup voltage in the data table is derived from
| the equation:
|  Vtable = Vcc - Voutput
| For the 8.3V in the table, it is actually 8.3V below Vcc and -5V
| with respected to Ground.
|*****************************************************************
|
[Pullup]
| voltage  I(typ)  I(min)  I(max)
|
 8.3V   -1410mA  -976.25mA -1992.8mA
 4.3V  -79.8mA  -55.6mA  -229.06mA
```

271329-F6

```
 3.3V   -47.1mA  -40.80mA -72.66mA
 2.8V   -46.1mA  -29.42mA -70.96mA
 2.3V   -44.8mA  -28.64mA -68.34mA
 1.8V   -42.1mA  -27.14mA -61.94mA
 1.3V   -35.1mA  -23.34mA -50.34mA
 0.8V  -24.1mA  -16.08mA -33.08mA
 0.3V   -9.5mA   -6.3mA  -12.86mA
 -0.2V   6.5mA   4.76mA  9.02mA
 -0.7V   24.3mA   17.3mA  33.04mA
 -1.2V   41.7mA   30.48mA  55.6mA
 -1.7V   56.4mA   42.26mA  74.14mA
 -2.2V   67.3mA   51.26mA  88.4mA
 -2.7V   74.6mA   56.96mA  96.58mA
 -3.7V   79.8mA   61.33mA  104.5mA
 -6.7V   82.4mA   63.55mA  109.5mA
|
[GND_clamp]
|
| Voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  -0.2mA  NA  NA
 -0.6V  -1.1mA  NA  NA
 -0.7V  -3.0mA  NA  NA
 -0.8V  -6.0mA  NA  NA
 -0.9V  -11.0mA  NA  NA
 -1.0V  -30.0mA  NA  NA
 -1.2V  -120.0mA NA  NA
 -2.0V  -180.0mA NA  NA
 -5.0V  -420.0mA NA  NA
|
|*********************************************************************
|  The data in the following POWER_clamp table is listed
| as "Vcc-relative", meaning that the voltage values are
| referenced to the Vcc pin.  The voltages in the data tables
|  are derived from the equation:
|   Vtable = Vcc - Voutput
| In this case, assuming that Vcc  is referenced to 3.3V.
| 0V in the table actually means 3.3V with respected to
| Ground and 0V above Vcc.
|*********************************************************************
|
[POWER_clamp]
| voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  0mA  NA  NA
 -0.6V  0mA  NA  NA
 -0.7V  0.1mA  NA  NA
 -0.8V  1.0mA  NA  NA
 -0.9V  8.0mA  NA  NA
 -1.0V  14.0mA  NA  NA
 -2.0V  100mA  NA  NA
|
|*********************************************************************
|
```

271329-F7

```
[Ramp]
|  typ  min  max
dV/dt_r  1.13/0.749n 0.93/0.868n 1.35/0.642n
dV/dt_f  0.99/0.447n 0.75/0.543n 1.27/0.387n
|
|*********************************************************************
|
[Model]  I/O3
Model_type I/O
Polarity Non-Inverting
Enable  Active-Low
Vinl = 0.8v
Vinh = 2.0v
|
|signal  ABUS<31:4>
|
|  typ min max
C_comp  2.9pF 2.9pF 2.9pF
[Voltage range]  3.3V 3.0V 3.6V
|
|*********************************************************************
|
[Pulldown]
| voltage  I(typ)  I(min)  I(max)
 -5.0V   -960.0mA  -580.0mA  -1410mA
 -2.0V   -190.0mA  -99.0mA  -292.0mA
 -1.0V   -21.0mA  -16.7mA  -27.1mA
 -0.5V   -13.30mA  -8.7mA   -20.5mA
 0.0V   0.0   0.0   0.0
 0.5V   12.9mA   8.3mA   20.1mA
 1.0V   23.7mA   15.1mA   37.2mA
 1.5V   31.5mA   19.7mA   49.7mA
 2.0V   35.4mA   21.6mA   56.6mA
 2.5V   36.3mA   22.0mA   58.6mA
 3.0V   36.6mA   22.2mA   59.0mA
 3.5V   36.9mA   22.3mA   59.4mA
 4.0V   37.0mA   22.4mA   59.7mA
 4.5V   37.1mA   22.5mA   59.8mA
 5.0V   37.2mA   22.5mA   60.0mA
 6.0V   37.2mA   22.5mA   60.0mA
 10.0V   37.2mA   22.5mA   60.0mA
|
|*****************************************************************
| Note that the pullup voltage in the data table is derived from
| the equation:
|  Vtable = Vcc - Voutput
| For the 8.3V in the table, it is actually 8.3V below Vcc and -5V
| with respected to Ground.
|*****************************************************************
|
[Pullup]
| voltage  I(typ)  I(min)  I(max)
|
 8.3V   -1410mA  -976.25mA -1992.8mA
 4.3V  -79.8mA  -55.6mA  -229.06mA
 3.3V   -47.1mA  -40.80mA -72.66mA
```

271329-F8

```
 2.8V   -46.1mA  -29.42mA -70.96mA
 2.3V   -44.8mA  -28.64mA -68.34mA
 1.8V   -42.1mA  -27.14mA -61.94mA
 1.3V   -35.1mA  -23.34mA -50.34mA
 0.8V  -24.1mA  -16.08mA -33.08mA
 0.3V   -9.5mA   -6.3mA  -12.86mA
 -0.2V   6.5mA   4.76mA  9.02mA
 -0.7V   24.3mA   17.3mA  33.04mA
 -1.2V   41.7mA   30.48mA  55.6mA
 -1.7V   56.4mA   42.26mA  74.14mA
 -2.2V   67.3mA   51.26mA  88.4mA
 -2.7V   74.6mA   56.96mA  96.58mA
 -3.7V   79.8mA   61.33mA  104.5mA
 -6.7V   82.4mA   63.55mA  109.5mA
|
[GND_clamp]
|
| Voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  -0.2mA  NA  NA
 -0.6V  -1.1mA  NA  NA
 -0.7V  -3.0mA  NA  NA
 -0.8V  -6.0mA  NA  NA
 -0.9V  -11.0mA  NA  NA
 -1.0V  -30.0mA  NA  NA
 -1.2V  -120.0mA NA  NA
 -2.0V  -180.0mA NA  NA
 -5.0V  -420.0mA NA  NA
|
|*********************************************************************
|  The data in the following POWER_clamp table is listed
| as "Vcc-relative", meaning that the voltage values are
| referenced to the Vcc pin.  The voltages in the data tables
|  are derived from the equation:
|   Vtable = Vcc - Voutput
| In this case, assuming that Vcc  is referenced to 3.3V.
| 0V in the table actually means 3.3V with respected to
| Ground and 0V above Vcc.
|*********************************************************************
|
[POWER_clamp]
| voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  0mA  NA  NA
 -0.6V  0mA  NA  NA
 -0.7V  0.1mA  NA  NA
 -0.8V  1.0mA  NA  NA
 -0.9V  8.0mA  NA  NA
 -1.0V  14.0mA  NA  NA
 -2.0V  100mA  NA  NA
|
|*********************************************************************
[Ramp]
|  typ  min  max
```

271329-F9

```
dV/dt_r  1.13/0.749n 0.93/0.868n 1.35/0.642n
dV/dt_f  0.99/0.447n 0.75/0.543n 1.27/0.387n
|
|*********************************************************************
|
[Model]  Input1
Model_type Input
Polarity Non-Inverting
Enable  Active-Low
Vinl = 0.8v
Vinh = 2.0v
|signal  A20M#,AHOLD,BOFF#,BRDY#,BS16#,BS8#,FLUSH#,
|  HOLD,IGNNE#,INTR,KEN#,NMI,RDY#,RESET,SRESET,SMI#,STPCLK#
|  typ  min  max
C_comp  2.0pF  2.0pF  2.0pF
[Voltage range]  3.3V 3.0V 3.6V
|
|*********************************************************************
|
[GND_clamp]
| Voltage  I(typ)  I(min)  I(max)
|
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  -0.2mA  NA  NA
 -0.6V  -1.1mA  NA  NA
 -0.7V  -3.0mA  NA  NA
 -0.8V  -6.0mA  NA  NA
 -0.9V  -11.0mA  NA  NA
 -1.0V  -30.0mA  NA  NA
 -1.2V  -120.0mA NA  NA
 -2.0V  -180.0mA NA  NA
 -5.0V  -420.0mA NA  NA
|
|*********************************************************************
|  The data in the following POWER_clamp table is listed
| as "Vcc-relative", meaning that the voltage values are
| referenced to the Vcc pin.  The voltages in the data tables
|  are derived from the equation:
|   Vtable = Vcc - Voutput
| In this case, assuming that Vcc  is referenced to 3.3V.
| 0V in the table actually means 3.3V with respected to
| Ground and 0V above Vcc.
|*********************************************************************
|
[POWER_clamp]
| voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  0mA  NA  NA
 -0.6V  0mA  NA  NA
 -0.7V  0.1mA  NA  NA
 -0.8V  1.0mA  NA  NA
 -0.9V  8.0mA  NA  NA
 -1.0V  14.0mA  NA  NA
 -2.0V  100mA  NA  NA
```

271329-G0

```
|
|*******************************************************************************
|
[Model]  Clockbuffer
Model_type Input
Polarity Non-Inverting
Enable  Active-Low
Vinl = 0.8V
Vinh = 2.0V
|signal  CLK
|  typ  min  max
C_comp  2.0pF  2.0pF  2.0pF
[Voltage range]  3.3V 3.0V 3.6V
|
|*******************************************************************************
|
[GND_clamp]
| Voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  -0.2mA  NA  NA
 -0.6V  -1.1mA  NA  NA
 -0.7V  -3.0mA  NA  NA
 -0.8V  -6.0mA  NA  NA
 -0.9V  -11.0mA  NA  NA
 -1.0V  -30.0mA  NA  NA
 -1.2V  -120.0mA NA  NA
 -2.0V  -180.0mA NA  NA
 -5.0V  -420.0mA NA  NA
|
|*******************************************************************************
|  The data in the following POWER_clamp table is listed
| as "Vcc-relative", meaning that the voltage values are
| referenced to the Vcc pin.  The voltages in the data tables
|  are derived from the equation:
|   Vtable = Vcc - Voutput
| In this case, assuming that Vcc  is referenced to 3.3V.
| 0V in the table actually means 3.3V with respected to
| Ground and 0V above Vcc.
|*******************************************************************************
|
[POWER_clamp]
| voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  0mA  NA  NA
 -0.6V  0mA  NA  NA
 -0.7V  0.1mA  NA  NA
 -0.8V  1.0mA  NA  NA
 -0.9V  8.0mA  NA  NA
 -1.0V  14.0mA  NA  NA
 -2.0V  100mA  NA  NA
|
|*******************************************************************************
|
[End]
```

271329-G1